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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/712,594	11/12/2003	Kouji Fujiyoshi	RYUKA.002AUS	8987

7590 07/01/2005  
MURAMATSU & ASSOCIATES  
Suite 225  
7700 Irvine Center Drive  
Irvine, CA 92618

EXAMINER

COLEMAN, WILLIAM D

ART UNIT PAPER NUMBER

2823

DATE MAILED: 07/01/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

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<b>Office Action Summary</b>	Application No. 10/712,594	Applicant(s) FUJIYOSHI ET AL.	
	Examiner W. David Coleman	Art Unit 2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 18 April 2005.  
 2a) ☐ This action is FINAL.                      2b) ☒ This action is non-final.  
 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-26 is/are pending in the application.  
 4a) Of the above claim(s) 9-12 and 27 is/are withdrawn from consideration.  
 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
 6) ☒ Claim(s) 1-8, 13-20 and 22-26 is/are rejected.  
 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
     Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
     Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
 a) ☒ All    b) ☐ Some \*    c) ☐ None of:  
     1. ☐ Certified copies of the priority documents have been received.  
     2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
     3. ☒ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
 \* See the attached detailed Office action for a list of the certified copies not received.

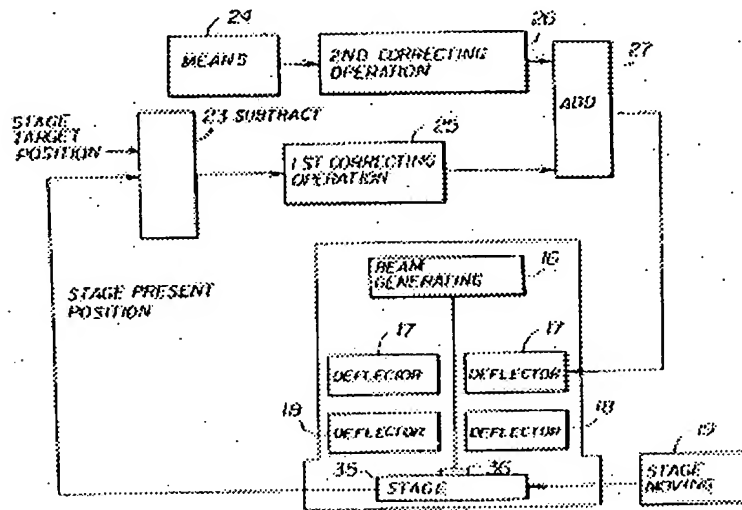
**Attachment(s)**

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)  | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>11/03</u> . | 6) <input type="checkbox"/> Other: _____  |

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**DETAILED ACTION*****Election/Restrictions***

1. Applicant's election without traverse of Group I invention, claims 1-8, 13-20 and 22-26 in the reply filed on April 18, 2005 is acknowledged.

***Claim Rejections - 35 USC § 102***

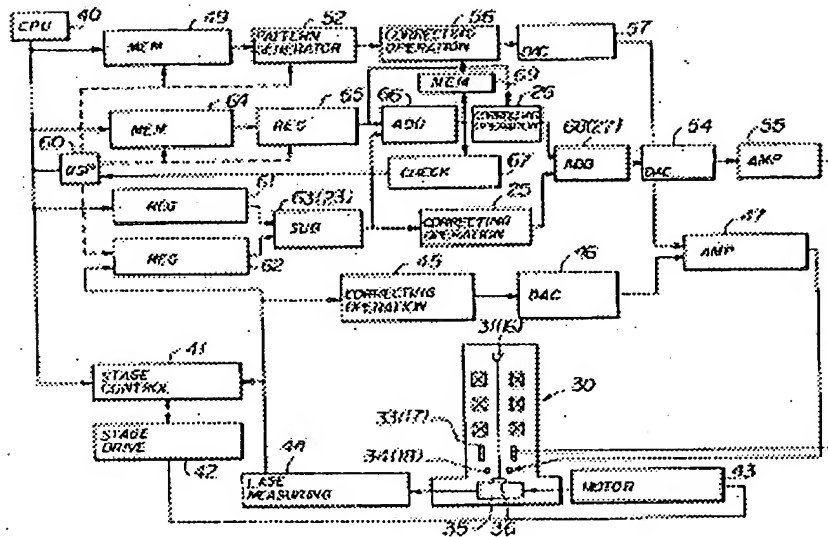
2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-8, 13-20 and 22-26 are rejected under 35 U.S.C. 102(b) as being anticipated by Kai et al., U.S. Patent 5,329,130.

4. Kai discloses a electron beam exposure apparatus substantially as claimed. See **FIGS. 1-11**, where Kai teaches the following limitations.



5. Pertaining to claim 1, Kai teaches an electron beam exposure apparatus for exposing a wafer by an electron beam, comprising:

a general control section 40 for controlling the electron beam exposure apparatus 30 collectively;

a first buffer memory **49** for temporarily storing exposure data, which is data of an exposure pattern **101**(see FIG. 9) to be formed on the wafer;

a second buffer memory 64 for temporarily storing the exposure data;

a first exposure section for applying the electron beam to the wafer based on the exposure data output from said first buffer memory; and

a first comparing section **25** for comparing the exposure data output from said first buffer memory with the exposure data output from said second buffer memory **26**, and for notifying the comparison result to said general control section (i.e., cpu).

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6. Pertaining to claim 2, Kai teaches the electron beam exposure apparatus as claimed in claim 1, wherein said first comparing section notifies said general control section whether the exposure data output from said first buffer memory is consistent with the exposure data output from said second buffer memory as the comparison result, and said general control section stores the comparison result in association with an exposure area to be exposed based on the exposure data.

7. Pertaining to claim 3, Kai teaches the electron beam exposure apparatus as claimed in claim 1, wherein said first comparing section compares the exposure data output from said first buffer memory with the exposure data output from said second buffer memory bit by bit (since the CPU uses information in the bit format, this limitation is met).

8. Pertaining to claim 4, Kai teaches the electron beam exposure apparatus as claimed in claim 2, further comprising:  
a second exposure section for applying an electron beam to a different wafer from the wafer based on the exposure data output from said first buffer memory;  
a first pattern generation section **D1** for generating shot data, which is the exposure data output from said first buffer memory being split into shots;  
a second pattern generation section **D2** for generating shot data, which is the exposure data output from said first buffer memory being split into shots; and

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a second comparing section for comparing the shot data output from said first pattern generation section with the shot data output from said second pattern generation section, and for notifying the comparison result to said general control section.

9. Pertaining to claim 5, Kai teaches the electron beam exposure apparatus as claimed in claim 4, wherein said second comparing section notifies said general control section whether the shot data output from said first pattern generation section is consistent with the shot data output from said second pattern generation section as the comparison result, and said general control section stores the comparison result notified from said second comparing section in association, with the comparison result notified from said first comparing section.

10. Pertaining to claim 6, Kai teaches the electron beam exposure apparatus as claimed in claim 1, further comprising a second exposure section for applying an electron beam to the different wafer based on the exposure data output from said second buffer memory.

11. Pertaining to claim 7, Kai teaches the electron beam exposure apparatus as claimed in claim 6, further comprising:

a first pattern correction section for correcting the shot data output from said first pattern generation section;

a second pattern correction section for correcting the shot data output from said second pattern generation section; and

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a third comparing section for comparing the shot data output from said first pattern correction section with the shot data output from said second pattern correction section, and for notifying the comparison result to said general control section.

12. Pertaining to claim 8, Kai teaches the electron beam exposure apparatus as claimed in claim 7, wherein said third comparing section notifies said general control section whether the shot data output from said first pattern correction section is consistent with the shot data output from said second pattern correction section as the comparison result, and said general control section stores the comparison result notified from said third comparing section in association with the comparison result notified from said first comparing section.

13. Pertaining to claim 13, Kai teaches an exposure apparatus for writing a desired exposure pattern to a wafer, comprising:

a buffer memory storing thereon exposure data, which is data of an exposure pattern to be formed on the wafer;

a comparing section for comparing a first exposure data output from said buffer memory based on a first control signal for exposing a first area with a second exposure data output from said buffer memory based on a second control signal for exposing a second area where the same exposure pattern as the first area is to be written; and

an error detection section for detecting, an error of the exposure pattern formed to the wafer based on the comparison result by said comparing section.

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14. Pertaining to claim 14, Kai teaches the exposure apparatus as claimed in claim 13, further comprising a first expect memory storing thereon the first exposure data output from said buffer memory, wherein said comparing section compares the first exposure data output from said first expect memory with the second exposure data output from said buffer memory.

15. Pertaining to claim 15, Kai teaches the exposure apparatus as claimed in claim 14, wherein said comparing section compares the first exposure data output from said first expect memory with the second exposure data output from said buffer memory bit by bit.

16. Pertaining to claim 16, Kai teaches the exposure apparatus as claimed in claim 14, further comprising a comparison result storing section storing thereon information indicating whether the first exposure data and the second exposure data are the same as each other as a comparison result in association with identification information on the second area, wherein said error detection section detects an error of the exposure pattern formed to the wafer based on the comparison result stored on said comparison result storing section.

17. Pertaining to claim 17, Kai teaches the exposure apparatus as claimed in claim 16, wherein  
said comparing section compares the first exposure data output from said first expect memory with a third exposure data output from said buffer memory based on a third control signal for exposing a third area where the same exposure pattern as the first area is to be written,



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said comparison result storing section stores information indicating whether the first exposure data and the second exposure data are the same as each other, and information indicating whether the first exposure data and the third exposure data are the same as each other, as the comparison result, and

said error detection section judges that there is an error in the exposure pattern formed to the third area when the first exposure data and the second exposure data are the same as each other and the first exposure data differs from the third exposure data, and judges that there is an error in the exposure pattern formed to the first area when the first exposure data differs from the second exposure data and the first exposure data differs from the third exposure data.

18. Pertaining to claim 18, Kai teaches the exposure apparatus as claimed in claim 14, further comprising a wafer stage mounting thereon the wafer for exposing the wafer while said wafer stage is moving in a first direction and then changing the direction and moving in a second direction opposite from the first direction, wherein in case that said wafer stage changes the direction, the first exposure data output from said buffer memory is written to said first expect memory.

19. Pertaining to claim 19, Kai teaches the exposure apparatus as claimed in claim 14, further comprising a second expect memory storing thereon the second exposure data output from said buffer memory, wherein said comparing section compares the second exposure data output from said second expect memory with the third exposure data output from said buffer memory based

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on a third control signal for exposing a third area where the same exposure pattern as the first area is to be written.

20. Pertaining to claim 20, Kai teaches the exposure apparatus as claimed in claim 19, further comprising;

a first expect memory control section for causing the first exposure data to be written to said first expect memory while said buffer memory is outputting the first exposure data, for causing said comparing section to read the first exposure data from said first expect memory while said buffer memory is outputting the second exposure data, and for causing the third exposure data to be written to said first expect memory while said buffer memory is outputting the third exposure data; and

a second expect memory control section for causing the second exposure data to be written to said second expect memory while said buffer memory is outputting the second exposure data, and for causing said comparing section to read the second exposure data from said second expect memory while said buffer memory is outputting the third exposure data.

21. Pertaining to claim 22, Kai teaches an exposure apparatus for writing a desired exposure pattern to a wafer, comprising: a buffer memory storing thereon exposure data, which is data of the exposure pattern to be formed on the wafer;  
an expect data generating section for generating a first expect data, which is an expected value of the exposure data to be output from said buffer memory based on a first control signal for exposing a first area;

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a comparing section for comparing a first exposure data output from said buffer memory based on the first control signal with the first expect data generated by said expect data generating section; an exposure section for exposing the wafer based on the first exposure data output from said buffer memory; and

an error detection section for detecting an error of an exposure pattern formed to the wafer based on a comparison result by said comparing section.

22. Pertaining to claim 23, Kai teaches the exposure apparatus as claimed in claim 22, further comprising a first expect memory storing thereon the first expect data generated by said expect data generating section, wherein said comparing section compares the first expect data output from said first expect memory with the first exposure data output from said buffer memory.

23. Pertaining to claim 24, Kai teaches the exposure apparatus as claimed in claim 23, further comprising a wafer stage mounting thereon the wafer, wherein said wafer stage moves in a first direction, then changes the direction and moves to a second direction opposite from the first direction, said exposure section performs first exposure processing on the first area while said wafer stage is moving in the first direction and performs second exposure processing on the first area while said wafer stage is moving in the second direction, and the first expect data is written to said first expect memory between the first exposure processing and the second exposure processing.

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24. Pertaining to claim 25, Kai teaches the exposure apparatus as claimed in claim 23, further comprising a wafer stage mounting thereon the wafer, wherein said wafer stage moves in a first direction, then changes the direction and moves to a second direction opposite from the first direction, said exposure section performs second exposure processing on the first area while said wafer stage is moving in the second direction after it has performed first exposure processing on the first area while said wafer stage has been moving in the first direction, and the first expect data, which is generated by said expect data generating section, is written to said first expect memory during the first exposure processing.

25. Pertaining to claim 26, Kai teaches the exposure apparatus as claimed in claim 25, further comprising a second expect memory storing thereon second expect data to be output from said buffer memory based on a second control signal for exposing a second area, wherein said wafer stage changes the direction once again to the first direction after it has moved in the second direction, said exposure section performs third exposure processing on the second area while said wafer stage is moving in the first direction after performing the second exposure processing on the first area while said wafer stage has been moving in the second direction, said comparing section compares the first expect data output from said first expect memory during the second exposure processing with the first exposure data output from said buffer memory, and the second expect data, which is generated by said expect data generating section, is written to said second expect memory during the second exposure processing.

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*Conclusion*

26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to W. David Coleman whose telephone number is 571-272-1856.

The examiner can normally be reached on Monday-Friday 9:00 AM - 5:30 PM.

27. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

28. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



W. David Coleman  
Primary Examiner  
Art Unit 2823

WDC